IN THE CLAIMS:

Please add claims 30-36 as follows:

1 -29 (Canceled)

30. (New) A memory component comprising:

a random access memory array having a plurality of storage locations;

a timing input for receiving a timing signal which when activ toggles between first and second states at a periodic rate; and

circuitry, coupled to the timing input and to the random access memory array, for transferring data to the memory component in synchronism with the timing signal and for transferring the data to the random access memory array.

31. (New) The memory component of claim 30, wherein the random access memory array is a dynamic random access memory array.

32. (New) The memory component of claim 30, wherein said circuitry includes a shift register.

33. (New) The memory component of claim 30, wherein said circuitry includes a multiplexer.

34. (New) A memory component comprising:

a random access memory array having a plurality of storage locations;

a timing input for receiving a timing signal which when activ toggles between first and second states at a periodic rate; and

circuitry, coupled to the timing input and to the random access memory array, for receiving data from the random access memory array and for transferring the data from the memory component in synchronism with the timing signal.

35. (New) The memory component of claim 34, wherein the random access memory array is a dynamic random access memory array.

36. (New) The memory component of claim 34, wherein said circuitry includes a shift register.

37. (New) The memory component of claim 34, wherein said circuitry includes a multiplexer.

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